

# Statistical Based Link Insertion for Robust Clock Network Design \*

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## Abstract

We present a statistical based non-tree clock distribution construction algorithm that starts with a tree and incrementally insert cross links, such that the skew variation of the final clock network is within a certain confidence interval under variations in wire width. Monte Carlo simulations show that the robustness of the final clock network can be significantly improved with a small increase in wire length.

## 1 Introduction

As the minimum feature sizes of VLSI circuits get smaller while the clock frequency increases, the effects of process variations on clock skews become significant. In [11], it is shown that interconnect variations in clock trees can cause as much as 25% variation in clock skew.

To counter the effects of skew variations, two categories of approaches have been proposed. One is the optimization on clock trees [18] [13]. These works perform wire sizing to minimize the skew variations.

The other category is the construction of hybrid non-trees, or in general, clock networks [16, 10, 15, 14]. The main reasoning behind this approach is to provide additional paths for the signal to reach the clock sink nodes such that the variations can be compensated. In [10], a center fat wire is used. The idea behind the center fat wire is that if clock signals from a tree arrive at multiple evenly distributed locations at the center chunk, the clock skew within the fat wire is negligible. In [16], a top (root) level mesh drives multiple clock trees in the lower (leaf) level. In [15], a top level tree drives a mesh in the lower level. In [14], cross links are added to convert a clock tree to a non-tree.

The main objective of the above works is to minimize the skew between clock sinks by performing optimizations that is based on computing the exact skew using delay models. However, process variations are statistically distributed and maybe spatially correlated. Therefore, it is advantageous to perform clock tree optimizations that are based on statistical information of the process variations. It is shown in [14] that inserting links to a clock network can reduce the skew variability without a significant increase in wirelength. In this work we utilize the concept of link insertion to increase the robustness of the clock network. The problem can be stated as follows: *Given a clock tree that satisfies the skew constraints between the clock sinks, successively insert links to the tree/network such that the skew variation is within a certain confidence interval, under variations in wire width.*

We propose an incremental statistical based optimization approach to increase the robustness of a clock distribution network to process variation by the addition of cross links [14]. We use statistical timing analysis [5, 2] to obtain the statistical distribution of the skew of the clock distribution network to determine the optimal insertion point. Once the cross links are inserted, the statistical skew distributions are updated before more links are inserted. In [14], the statistical skew analysis is performed only at the final step, when all links have been added. Monte Carlo simulations show that the robustness of the final clock network can be increased with a small increase in wire length. In this work, we use a fitted Elmore delay model [1] and apply this to the Elmore delay computation of both clock trees and non-trees.

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## 2 Statistical Distribution of Parameters

Consider a wire of two segments.  $e_i$  has a uniform width of  $w_i$  and of length  $l_i$ .  $e_j$  has a width of  $w_j$  and of length  $l_j$ . If we use a RC  $\pi$ -type circuit to model this wire and evaluate the Elmore delay of the wire from one end of  $e_i$  (source node) to the end of  $e_j$ , we have:

$$d_j = \frac{r_{\square} l_i}{w_i} \left( \frac{c_a l_i w_i}{2} + \frac{c_f l_i}{2} + c_a l_j w_j + c_f l_j \right) + \frac{r_{\square} l_j}{w_j} \left( \frac{c_a l_j w_j}{2} + \frac{c_f l_j}{2} \right), \quad (1)$$

where  $r_{\square}$  is the wire resistance per unit square,  $c_a$  is the area capacitance per unit length and  $c_f$  is the fringing capacitance per unit length.

The Elmore delay model has been widely used because it is extremely efficient to compute and has a good fidelity with respect to HSPICE simulation [3]. The primary disadvantage of it is that it has limited accuracy and it always overestimates the delay [8]. To increase the accuracy, we use a fitted Elmore delay model [1] in this work, although we refer to it as Elmore delay throughout the paper.

Due to process variations, the width of a fabricated wire may deviate from the designed width and it would follow a statistical distribution. Therefore, we replace all occurrences of  $w_i$  and  $w_j$  with random variables (RV)  $W_i$  and  $W_j$  and express the Elmore delay of the wire as another RV denoted as  $D_j$ :

$$D_j = \left[ \frac{r_{\square} c_a l_i^2}{2} + \frac{r_{\square} c_a l_j^2}{2} \right] + \left[ \frac{r_{\square} c_f l_i}{2} + r_{\square} c_f l_j \right] \left( \frac{1}{W_i} \right) + \left[ \frac{r_{\square} c_f l_j}{2} \right] \left( \frac{1}{W_j} \right) + [r_{\square} c_a l_i l_j] \left( \frac{W_j}{W_i} \right). \quad (2)$$

We assume that  $W$  has a normal distribution with mean ( $\bar{W}$ ) and standard deviation ( $\sigma_W$ ). In this work, we consider only wire width variations, but it can be extended to handle other sources of variations such as wire height.

Using a Taylor series expansion of Eqn. (1) up to the second order, we can approximate  $D_j$  with:

$$\hat{D}_j = d_0 + \sum_{k=1}^m \frac{\partial D_j}{\partial W_k} \bigg|_{W_k = \bar{W}_k} \Delta W_k + \frac{1}{2} \sum_{k_1=1}^m \sum_{k_2=1}^m \frac{\partial^2 D_j}{\partial W_{k_1} \partial W_{k_2}} \bigg|_{W_{k_1} = \bar{W}_{k_1}, W_{k_2} = \bar{W}_{k_2}} \Delta W_{k_1} \Delta W_{k_2}, \quad (3)$$

where  $d_0 = d_j$ , evaluated at the expansion point (which is the Elmore delay if we do not consider process variations),  $m$  is the number of RVs involved in Eqn. (2), and  $\Delta W_k = W_k - \bar{W}_k$ .  $\hat{D}_j$  is in the form:

$$\hat{D}_j = d_j + \sum_{k=1}^m a_k \Delta W_k + \sum_{k_1=1}^m \sum_{k_2=1}^m b_{k_1 k_2} \Delta W_{k_1} \Delta W_{k_2}, \quad (4)$$

where  $a_k$  and  $b_{k_1 k_2}$  are scalar constants. To find the mean and the variance of Eqn. (4), we have:

$$E(\hat{D}_j) = d_j + \sum_{k=1}^m a_k E(\Delta W_k) + \sum_{k_1=1}^m \sum_{k_2=1}^m b_{k_1 k_2} E(\Delta W_{k_1} \Delta W_{k_2}), \quad (5)$$

$$\text{Var}(\hat{D}_j) = \sum_{k_1=1}^m \sum_{k_2=1}^m a_{k_1} a_{k_2} E(\Delta W_{k_1} \Delta W_{k_2}) + H.O.T., \quad (6)$$

where  $E(\Delta W_{k_1} \Delta W_{k_2})$  is the covariance between  $\Delta W_{k_1}$  and  $\Delta W_{k_2}$  (since both  $\Delta W_{k_1}$  and  $\Delta W_{k_2}$  have zero mean). *H.O.T.* are higher order terms. In this work, we do not consider *H.O.T.* for variance computation. The  $m$  RVs are assumed to be spatially correlated and is given in a covariance matrix of size  $m \times m$  [5, 2]. Therefore, with the mean values of each RV, we can easily compute the mean and variance of the delay of the wire.

For a clock tree, we denote the skew between any two nodes  $i$  and  $j$  to be  $q_{ij} = d_i - d_j$ . Therefore, we can approximate  $Q_{ij} = D_i - D_j$  with  $\hat{Q}_{ij} = \hat{D}_i - \hat{D}_j$ :

$$\hat{Q}_{ij} = q_{ij} + \sum_{k=1}^m \tilde{a}_k \Delta W_k + \sum_{k_1=1}^m \sum_{k_2=1}^m \tilde{b}_{k_1 k_2} E(\Delta W_{k_1} \Delta W_{k_2}), \quad (7)$$

where  $\tilde{a}_k$  and  $\tilde{b}_k$  are the scalar constants obtained from  $\hat{D}_i - \hat{D}_j$ . Hence,  $E(\hat{Q}_{ij})$  and  $Var(\hat{Q}_{ij})$  can be computed in a similar fashion as in Eqn. (5) and (6). The mean and the variance can be found in  $O(m^2)$  run time (we do not use higher orders for variance computation).

To reduce the complexity of the mean and variance computation, we make use of Principal Component Analysis (PCA) [12] to convert the set of correlated RVs to an uncorrelated set as in [5]. In turn, we can express all the delays and skews with the new uncorrelated set of RVs. Since the cross terms no longer exist, there are only  $1 + 2m$  terms for every  $\hat{D}$  and  $\hat{Q}$ . Therefore, the mean and variance can now be found in  $O(m)$  run time. For the rest of the paper,  $\hat{D}$ 's and  $\hat{Q}$ 's are assumed to be expressed with the new uncorrelated set of RVs.

### 3 Statistical Delay and Skew

A challenge of adding links to trees is that once a link is added to form a non-tree, Eqn. (1) and consequently Eqn. (4) can no longer be used directly to compute the delays. Suppose that  $n$  is the number of nodes in the clock tree. In general, given the node conductance matrix  $G$  of size  $n \times n$ , and the nodal capacitance matrix  $C$  that is of size  $n \times 1$ , the RC delay can be found by computing  $G^{-1}C$  or  $\mathcal{R}C$ , where  $\mathcal{R} = G^{-1}$ .

In this work, a wire that passes through multiple grids is treated as a path  $p$  of multiple nodes and edges. The capacitance ( $c_L$ ) and resistance ( $r_L$ ) of the wire can be expressed as:

$$c_L = \sum_{i \in \text{path } p} l_i (c_a W_i + c_f), \quad \text{and} \quad r_L = r_{\square} \sum_{i \in \text{path } p} \frac{l_i}{W_i}.$$

We can express  $c_L$  and  $r_L$  in the form of a Taylor series expansion similar to Eqn. (4), then represent them with a set of uncorrelated RVs obtained by PCA. To avoid adding new notation, we again use  $r_L$  and  $c_L$  to denote resistance and capacitance expressed in terms of the set of uncorrelated RVs. To find the conductance, we take the Taylor series expansion of  $\frac{1}{r_L}$  and represent it with a set of uncorrelated RVs. The remaining challenge is in computing  $\mathcal{R}C$  and updating it as successive links are inserted.

#### 3.1 Incremental Updates

Suppose the  $x^{\text{th}}$  link wire that we add to the tree has a resistance of  $r_x$  and a capacitance of  $c_x$  and the link wire is added between nodes  $i$  and  $j$ .

Updating  $C$  is trivial. We simply add  $\frac{c_x}{2}$  to two entries of  $C$ , namely  $C_i$  and  $C_j$ . This can be viewed as adding a column vector ( $\Delta C_x$ ) to  $C$ :

$$C_x = C_{x-1} + \Delta C_x, \quad (8)$$

where:

$$\Delta C_x = \begin{bmatrix} c_1 \\ \vdots \\ c_n \end{bmatrix}, \quad c_k = \begin{cases} \frac{c_x}{2} & k = \{i, j\}, \\ 0 & \text{otherwise.} \end{cases} \quad (9)$$

In this work, we do not construct  $\mathcal{R}$ . However, to illustrate the concept of updating  $\mathcal{R}C$ , assume that it is given. One way to update  $\mathcal{R}$  is by adding  $\frac{1}{r_x}$  to the appropriate entries of  $G$ , and performing an inverse operation to obtain the new  $\mathcal{R}$ . If we observe the update of  $G$ , we see that adding a link resistance  $r_L$  between nodes  $i$  and  $j$  is equivalent to subtracting (adding) the link conductance  $\frac{1}{r_L}$  from (to) two entries of  $G$ , namely  $G_{ii}$ ,  $G_{jj}$  and adding

(subtracting)  $\frac{1}{r_L}$  to (from)  $G_{ij}$ ,  $G_{ji}$ . If we put these four link conductances in a matrix  $\Delta G$ , the new  $G$ , is given by:

$$G_x = G_{x-1} + \Delta G_x, \quad (10)$$

such that:

$$\Delta G_x = -\frac{1}{r_x} \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix} \underbrace{\begin{bmatrix} v_1 \cdots v_n \end{bmatrix}}_{V_x^T}, \quad v_k = \begin{cases} 1 & k = i, \\ -1 & k = j, \\ 0 & \text{otherwise,} \end{cases} \quad (11)$$

and we denote the vector of  $v$ 's as  $V_x$ . From Eqn. (11), we can see that  $\Delta G$  is a matrix of rank-one. Therefore, instead of performing an inverse computation of  $G_x$  after every link inserted, we perform a rank-one update on  $\mathcal{R}_{x-1} (G_{x-1}^{-1})$  to obtain  $\mathcal{R}_x (G_x^{-1})$  directly. The rank-one update of  $\mathcal{R}_{x-1}$  is given by [7]:

$$\mathcal{R}_x = [\mathcal{R}_{x-1} - \frac{1}{r_x} V_x V_x^T]^{-1} = \mathcal{R}_{x-1} + \beta \mathcal{R}_{x-1} V_x V_x^T \mathcal{R}_{x-1}, \quad (12)$$

where:

$$\beta = \frac{1}{r_x - V_x^T \mathcal{R}_{x-1} V_x}$$

By using a rank-one update, we can update  $\mathcal{R}$  after a link is inserted, without an inverse operation. The new delay of every node can then be obtained by multiplying  $\mathcal{R}$  with the updated  $C$ . This allows us to compute the statistical delay and skew of the updated clock network in  $O(mn^2)$  time. However, in this work, we are only interested in the product of  $\mathcal{R}$  and  $C$ . Therefore,  $\mathcal{R}$  is not constructed and it is not necessary to update  $\mathcal{R}$  and  $C$  separately. By directly obtaining and updating  $\mathcal{R}C$ , there is a reduction in computation complexity.

This approach is similar to [4] in a sense that they are also incrementally computing the new RC delay as resistive links are added back to a tree to compute the RC delay of the original network (the resistive links were removed from the original RC network to form a tree). However, in [4], their objective is to compute the final delay of a given RC network without the presence of variations. In this work, we are computing the statistical delays and skews in the presence of variations. We also add new capacitances to the network and therefore we have additional terms that we need to compute. The main concept behind our work is the use of a rank-one update and the use of the unique structure in  $\Delta G_x$  and  $\Delta C_x$ , for a direct update of the statistical delay.

### 4 Direct Incremental Statistical Delay Update

To compute and update  $\mathcal{R}C$  directly after a link is inserted, we have (from Eqns. (8), (10) and (12)):

$$\mathcal{R}_x C_x = \left[ \mathcal{R}_{x-1} + \frac{\mathcal{R}_{x-1} V_x V_x^T \mathcal{R}_{x-1}}{r_x - V_x^T \mathcal{R}_{x-1} V_x} \right] (C_{x-1} + \Delta C_x) \quad (13)$$

To compute  $\mathcal{R}_x C_x$ , we must obtain the following terms:

- $\mathcal{R}_{x-1} C_{x-1}$ : This term corresponds to the RC delay before the  $x^{\text{th}}$  link is inserted. When  $x = 1$ ,  $\mathcal{R}_0 C_0$  corresponds to the original Elmore delay of the clock tree (before the first link is inserted), which can be found by a bottom-up, top-down tree traversal in  $O(mn)$  time. This term is computed and stored for successive link insertions and requires  $O(mn)$  space complexity.
- $\mathcal{R}_{x-1} V_x$ : By replacing the  $x$ 's with  $y-1$  in the brackets and replacing  $(C_{x-1} + \Delta C_x)$  with  $V_x$  in Eqn. (13), this term can be computed using the recursive function:

$$\mathcal{R}_{y-1} V_x = \underbrace{\mathcal{R}_{y-2} V_x}_{(a)} + \underbrace{\frac{\mathcal{R}_{y-2} V_{y-1} V_{y-1}^T (\mathcal{R}_{y-2} V_x)}{r_{y-1} - V_{y-1}^T \mathcal{R}_{y-2} V_{y-1}}}_{(b)}. \quad (14)$$

$y$  is used to indicate the difference between the  $V$ 's of previous links that have been already added and the  $V$ 's of the last or current link. We compute  $\mathcal{R}_{y-2}V_x$  in (a) by doing recursive operations of Eqn. (14). This will generate a term similar to (b) and a term like (a) which will require further recursive operations. Eventually the term (a) will reach  $\mathcal{R}_0V_x$ . Note that this is very similar to  $\mathcal{R}_0C_0$ , which is the Elmore delay of the original tree. Therefore, we can treat  $\mathcal{R}_0V_x$  as the Elmore delay of a special tree that has the same exact topology and resistance values as the original tree. However, the tree has zero node capacitances except for node  $i$  and node  $j$ . These two nodes have a "capacitance" of 1 and  $-1$  respectively when the  $x^{\text{th}}$  link is inserted.

The term  $\mathcal{R}_{y-2}V_{y-1}$  (or  $\mathcal{R}_{y-2}V_{x-1}$ ) in (b) has been computed in the  $(x-1)^{\text{th}}$  link and is known since we store this term from the previous link insertions. Since  $\mathcal{R}_{y-1}$  is symmetric,  $(V_x^T \mathcal{R}_{y-1}) = (\mathcal{R}_{y-1}V_x)^T$ . The product of  $V_{y-1}^T$  (Eqn. (11)) and  $\mathcal{R}_{y-2}V_{y-1}$  can be easily found by taking the difference between the  $i^{\text{th}}$  the  $j^{\text{th}}$  entry of  $\mathcal{R}_{y-2}V_{y-1}$  and can be done in  $O(m)$  run time. Therefore, (b) can be computed as soon as  $\mathcal{R}_{y-2}V_x$  (or (a)) is obtained.

Once  $\mathcal{R}_{y-1}V_x$  is computed, it is stored for successive link insertions and requires  $O(mm)$  space complexity. Note that we store terms that are  $\mathcal{R}_{y-1}V_x$ , i.e., where the index differs by one. The rest are not stored because they are not reused again in future link insertions.

- $\mathcal{R}_{y-1}\Delta C_x$ : The method of computing this term is similar to finding  $\mathcal{R}_{y-1}V_x$ . It will require recursive operations similar to Eqn. (14), except  $V_x$  is replaced with  $\Delta C_x$ .  $\mathcal{R}_0\Delta C_x$  can be found by computing the Elmore delay of a special tree has zero node capacitances except for node  $i$  and node  $j$ . These two nodes both have a capacitance of  $\frac{c_x}{2}$  when the  $x^{\text{th}}$  link is inserted.

$V_x^T \mathcal{R}_{y-1}\Delta C_x$  can be computed in  $O(m)$  as soon as  $\mathcal{R}_{y-1}\Delta C_x$  is obtained.  $\mathcal{R}_{y-1}\Delta C_x$  is not stored for successive link insertions.

In [4], no new capacitances are added when the links are added back to form the original RC network. In this work, we have the extra term  $\mathcal{R}_0\Delta C_x$ , which is computed simultaneously with  $\mathcal{R}_0V_x$  via Elmore delay computation of special trees. The other difference is in the space complexity. Using the same notation, [4] requires  $O(mnx^2)$ . In this work, we require  $O(mnx)$  to store the terms  $\mathcal{R}_{y-2}V_{x-1}$  and  $\mathcal{R}_yC_x$ .

## 5 Statistical based link selection

In a synchronous circuit, between every pair of sinks, say  $i$  and  $j$ , there are two inequalities that pose lower and upper bound constraints on the skew  $q_{ij}$  [6]. These are the hold time and setup time constraints. For simplicity, we use  $a_{ij} \leq q_{ij} \leq b_{ij}$  to represent the lower and upper bound skew constraints between sinks  $i$  and  $j$ .

The objective of this work is to achieve:

$$a_{ij} + \alpha\sigma_{ij} \leq q_{ij} \leq b_{ij} - \alpha\sigma_{ij}, \quad (15)$$

where  $\alpha\sigma_{ij}$  is  $\alpha$  times the standard deviation of  $Q_{ij}$  and  $\sigma_{ij}$  is obtained from the statistical skew analysis. In other words, we would like the mean of the skew of every sink pair to be adjusted such that the  $2\alpha\sigma_{ij}$  skew variation ( $\mu \pm \alpha\sigma_{ij}$ ) for that particular pair of sinks lies within their skew constraints. A skew violation occurs when the skew constraints are not satisfied. In this work, we assume  $\alpha = 3$ .

In Section 4, we showed that we can obtain the statistical delay and skew after a link has been inserted. Therefore, for any candidate link, we can temporarily insert the link, perform a statistical delay evaluation and check against the skew constraints for skew violations. We can then determine whether that candidate link should be permanently inserted to resolve the skew violations. Once the link is inserted, the delay and skew is updated and is ready for the next link to be inserted. The algorithm is summarized in Fig. 1.

### 5.1 Candidate link selection

In a clock tree with  $n$  nodes, there are  $O(n^2)$  pairs of nodes that could be considered as candidates. We can reduce the search space by setting a limit on the link distance. The reason for this is that we would like to keep

<b>Input:</b> Clock tree $\mathcal{T}$ , skew constraints (or bounded skew), grids and Covariance matrix
<b>Output:</b> Clock network $\tilde{\mathcal{T}}$
1. Add internal nodes to $\mathcal{T}$ based on the grid partition
2. Perform PCA to obtain uncorrelated set of RVs
3. Perform statistical skew analysis on $\mathcal{T}$
4. While skew violation exists: (See Eqn. (15))
a. For each sink pair considered for link sink insertion, find the worst case skew violation
b. Insert the link that has the best worst case violation
c. Update skew

Fig. 1: Statistical link insertion algorithm

the links as short as possible to minimize the total wirelength. A longer wirelength imposes a larger load to the clock driver and will consume more power per switching cycle. The other reason is that a shorter link inserted will have a smaller perturbation on the delay and skew of the overall tree because a shorter link would have smaller link capacitances. We can see this from the computation of  $\mathcal{R}_0\Delta C_x$ .

One other constraint that we use is to limit the height of the subtree that is rooted at the nearest common ancestor of the two nodes where the link is to be inserted. From the computation of  $\mathcal{R}_0V_x$ , we can see that the taller the subtree, the larger the effect the link has on the tree.

The overall time to insert the  $x^{\text{th}}$  link, update  $\mathcal{R}_yC_x$  followed by a statistical skew evaluation takes  $O(mn^2 + xmn + nm)$  time. Assuming for the link selection process, we consider  $h$  candidate pairs of nodes as the  $x^{\text{th}}$  link inserted. Therefore, for a total of  $x$  links, the run time complexity of our algorithm is  $O(x(h(mn^2 + xmn + nm)))$ .

## 6 Experiments and Results

The proposed statistical link insertion algorithm has been implemented in Matlab and tested on three ISCAS89 benchmark circuits on a Sun UltraSparc-II workstation. The wires are assumed to have a resistance of  $0.03\Omega$  per unit square, an area capacitance of  $1fF/\mu m$  and a fringing capacitance of  $1.2fF/\mu m$ . These numbers are typical for a  $0.18\mu m$  process technology.

To truly evaluate the quality of our solution we performed Monte Carlo simulations on the original clock tree and the final clock tree with inserted links. We assume that the process variations are spatially correlated. We use a grid partitioning to section the die into a number of grids ( $m$ ). Given the clock tree, we first add additional internal nodes to the tree based on the grid partitioning.

In these experiments, the clock tree (network) is fed into the simulator and wire widths are assigned to all the edges, while retaining the topology. The assignment of wire widths follows a normal distribution that has a mean of  $w_{mean}$  and a standard deviation of  $\sigma_w$ . The  $3\sigma_w$  variation of the wire widths in every grid has been set to an arbitrary value of  $\pm 20\%$  of the nominal value. In other words, the minimum ( $-3\sigma$ ) is set at 80% of the nominal value and the maximum ( $+3\sigma$ ) is set at 120% of the nominal value. The skews between all pairs of sinks are evaluated based on this width assignment using a linear interconnect simulator [9]. For each clock tree, 2000 simulations are performed with a new set of width assignment for every simulation.

Table 1 shows the comparison of statistical skew analysis (using fitted Elmore and without) with Monte Carlo simulation. *Max mean skew* is defined as the largest mean skew in the circuit and *Max SD skew* is the largest standard deviation of skew in the circuit.  $\Delta$  *Max mean skew* ( $\Delta$  *Max SD skew*) is to show the difference of using statistical analysis versus Monte Carlo simulations when computing *Max mean skew* (*Max SD skew*). The results show that there is an increased accuracy when fitted Elmore delay is used for non-trees. Table 2 shows the Monte Carlo skew analysis on the clock trees before links are inserted. It shows the number of clock sinks, the wirelength, the maximum of the mean of all skews and the maximum of the standard deviation of all skews. The trees are generated using the UST/DME clock routing algorithm [17] with different safety margins. The idea of safety margins is to push the clock skew away from the bounds during clock routing such that they provide an increased tolerance to process variations. This, however, increases the wirelength. For each circuit, we increase its safety margin at  $100ps$  intervals until a 100% yield is achieved. The yield is defined as the percentage of clock trees/networks tested in the simulations that meet all skew constraints under the presence of process

Table 1: Comparison of statistical skew analysis with Monte Carlo (MC) simulations for non-trees

Benchmark Circuit				(MC)		Stat. analysis (SA)		$\Delta = \frac{SA-MC}{MC}$		(*SA)		$\Delta = \frac{*SA-MC}{MC}$	
Circuit	Clock pins #	Nodes #	Grids #	Max mean skew (ps)	Max SD skew (ps)	Max mean skew (ps)	Max SD skew (ps)	$\Delta$ Max mean skew (%)	$\Delta$ Max SD skew (%)	Max mean skew (ps)	Max SD skew (ps)	$\Delta$ Max mean skew (%)	$\Delta$ Max SD skew (%)
s1423	74	262	16	1053	21.1	1084	21.9	2.9	3.8	1241	25.4	17.9	20.4
s5378	179	594	64	945	103	942	110	-0.3	6.8	1055	128	11.6	24.3
s15850	597	2162	64	1841	453	1758	463	-4.5	2.2	2247	569	22.1	25.6

\*Without using fitted Elmore delay

Table 2: Monte Carlo skew and yield analysis before link insertion

Circuit	UST/DME Safety margin (ps)	Wire-length (mm)	Max mean skew (ps)	Max sd skew (ps)	Yield (%)
s1423	0	107.3	1119	22.4	0
	1500	141.2	1077	21.8	100
s5378	0	176.5	950	102	0
	400	363.5	941	101	100
s15850	0	448.6	1853	455	0
	300	1079.7	1821	451	100

Table 3: Monte Carlo skew and yield analysis after link insertion

Circuit	Max mean skew (ps)	Max mean skew change (%)	Max sd skew (ps)	Max sd skew change (%)	Wire-length (mm)	$\Delta$ Wire-length (%)	* $\Delta$ Wire-length (UST) (%)	Links inserted	CPU time (min)	Yield (%)
s1423	1053	-5.9	21.1	-1.3	119.1	10.9	-15.7	10	2.6	100
s5378	945	-0.5	103	1.0	185.7	5.2	-48.9	8	53.8	100
s15850	1841	-0.6	453	-0.4	503.3	12.2	-53.4	20	655	100

\*Comparing with UST/DME with 100% yield

variations, based on the  $6\sigma$  definition in Eqn. (15). We show in Table 2 the minimal safety margin and the increased wirelength for each circuit with 100% yield. Our algorithm starts with clock trees with zero safety margins.

The abrupt changes in the yield stems from the fact that the safety margin increments in the experiments are done in intervals. It would require very large amount of resources to run Monte Carlo simulations to determine the yield using fine safety margin increments. For the smallest benchmark circuit s1423, we had to increase the wire width variation to  $\pm 30\%$  to introduce a yield loss. This is because smaller clock trees typically has shorter branches and therefore are less affected by variations.

Table 3 shows the Monte Carlo skew analysis on the clock trees after the links are inserted. For each benchmark circuit, it shows the value and the percentage change in both the maximum mean skew and the maximum standard deviation of skew from the original clock tree with zero safety margins, the wirelength and the number of links inserted.  $\Delta$  wire-length (UST) is the wirelength difference between the final clock network obtained using our approach versus the clock tree obtained using the UST approach (that corresponds to a 100% yield). From the results, we see that we can increase the yield with a small number of links that do not significantly increase the wirelength. It shows a maximum increase of 12.2% in wirelength compared to the original tree.

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